REMARKS

Acceptance and formal entry therefor of this preliminarily submitted amendment prior to the Examiner taking up the above-identified application for a formal review is respectfully requested.

By the amendments presented hereinabove, originally submitted claims 1-15 are being substituted therefor with newly presented claims 16-28. The invention of new claims 16-28 is directed to a memory card including a substrate, a first semiconductor chip and a second semiconductor chip stacked over the main surface of the first semiconductor chip.

Specifically, in the memory card according to base claim 16, the substrate includes a plurality of electrodes on the main surface thereof and a plurality of external terminals on the rear surface thereof and, further, the first semiconductor chip of the pair of chips includes a memory circuit and has a plurality of bonding pads formed on the main surface thereof, furthermore, is mounted on the main surface of the substrate. The second semiconductor chip of the stacking arrangement includes a control circuit to control the memory circuit (of the first semiconductor chip) and has bonding pads formed on the main surface thereof and, also, the second chip is stacked over the main surface of the first semiconductor chip. The invention according to claim 16 further sets forth first wires electrically connecting respective ones of the bonding pads of the first semiconductor chip with corresponding ones of the plurality of electrodes (of the substrate) and second wires electrically connecting respective ones of the bonding pads of the second semiconductor chip with corresponding ones of the plurality of electrodes (on the main surface of the substrate). The memory card also calls for resin sealing the first and second semiconductor chips, the first and second plurality of wires and the plurality of electrodes.

The invention according to base claim 16 is further characterized in accordance with the corresponding dependent claims thereof. For example, with regard to claims 18, 24, 26 and 28, the memory circuit of the first semiconductor chip is a flash memory. According to another featured aspect of the invention, the first wires as well as the second wires are distributed in the manner which avoids any crossing over (overlapping) between respective ones of the first wires with respective ones of the second wires (see claim 17). This can be seen with regard to the various disclosed example embodiments described in the Specification and illustrated in the drawings. A further aspect of the invention concerns reducing the thickness of the stacked semiconductor chip arrangement through polishing the rear main surfaces of the respective semiconductor chips (See claims 19, 21 and 25). A still further aspect of the invention calls for the upper or second semiconductor chip in the stacking arrangement to have a smaller size than that of an underlying semiconductor chip in the stacking arrangement. An example of this can be seen with regard to the control chip 1B stacked on chips 1A in Figs. 7-8 or with regard to that shown in Figs. 11-12, the latter featuring a BGA type packaging scheme, as well as with regard to Fig. 13 of the drawings, although not limited thereto.

It is submitted, a clear line of demarcation exists between that of the claimed subject matter directed to the above newly submitted substitute claims with that of the claims of the two prior U.S. Patents corresponding to the prior, parent and grandparent applications in the line of continuing applications mentioned on page 1 of the present Specification.

Examination as well as favorable action therefor of the newly submitted substitute claims is respectfully requested.

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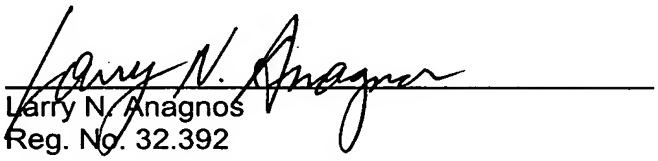
Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP



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